# Chapter 1 – Computer Systems Overview

**TRUE/FALSE QUESTIONS:**

1) The processor controls the operation of the computer and performs its data processing functions.

Answer: True False

2) It is not possible for a communications interrupt to occur while a printer interrupt is being processed.

Answer: True False

3) A system bus transfers data between the computer and its external environment.

Answer: True False

4) Cache memory is invisible to the OS.

Answer: True False

5) With interrupts, the processor can not be engaged in executing other instructions while an I/O operation is in progress.

Answer: True False

6) Digital Signal Processors deal with streaming signals such as audio and video.

Answer: True False

7) The fetched instruction is loaded into the Program Counter.

Answer: True False

8) Interrupts are provided primarily as a way to improve processor utilization.

Answer: True False

9) The interrupt can occur at any time and therefore at any point in the execution of a user program.

Answer: True False

10) Over the years memory access speed has consistently increased more rapidly than processor speed.

Answer: True False

11) An SMP can be defined as a stand-alone computer system with two or more similar processors of comparable capability.

Answer: True False

12) The Program Status Word contains status information in the form of condition codes, which are bits typically set by the programmer as a result of program operation.

Answer: True False

13) An example of a multicore system is the Intel Core i7.

Answer: True False

14) In a two-level memory hierarchy the Hit Ratio is defined as the fraction of all memory accesses found in the slower memory.

Answer: True False

15) The operating system acts as an interface between the computer hardware and the human user.

Answer: True False

**MULTIPLE CHOICE QUESTIONS:**

1) The four main structural elements of a computer system are:

A) Processor, Main Memory, I/O Modules and System Bus
B) Processor, I/O Modules, System Bus and Secondary Memory
C) Processor, Registers, Main Memory and System Bus
D) Processor, Registers, I/O Modules and Main Memory

Answer: A

2) The _____ holds the address of the next instruction to be fetched.

A) Accumulator (AC)
B) Instruction Register (IR)
C) Instruction Counter (IC)
D) Program Counter (PC)

Answer: D

3) The _____ contains the data to be written into memory and receives the data read from memory.

A) I/O address register
B) memory address register
C) I/O buffer register
D) memory buffer register

Answer: D

4) Instruction processing consists of two steps:

A) fetch and execute
B) instruction and execute
C) instruction and halt
D) fetch and instruction

Answer: A

5) The _____ routine determines the nature of the interrupt and performs whatever actions are needed.

A) interrupt handler
B) instruction signal
C) program handler
D) interrupt signal

Answer: A

6) The unit of data exchanged between cache and main memory is _____ .

A) block size B) map size C) cache size D) slot size

Answer: A

7) The _____ chooses which block to replace when a new block is to be loaded into the cache and the cache already has all slots filled with other blocks.

A) memory controller
B) mapping function
C) write policy
D) replacement algorithm

Answer: D

8) _____ is more efficient than interrupt-driven or programmed I/O for a multiple-word I/O transfer.

A) Spatial locality
B) Direct memory access
C) Stack access
D) Temporal locality

Answer: B

9) The _____ is a point-to-point link electrical interconnect specification that enables high-speed communications among connected processor chips.

A) QPI B) DDR3 C) LRUA D) ISR

Answer: A

10) Small, fast memory located between the processor and main memory is called:

A) Block memory
B) Cache memory
C) Direct memory
D) WORM memory

Answer: B

11) In a uniprocessor system, multiprogramming increases processor efficiency by:

A) Taking advantage of time wasted by long wait interrupt handling
B) Disabling all interrupts except those of highest priority
C) Eliminating all idle processor cycles
D) Increasing processor speed

Answer: A

12) The two basic types of processor registers are:

A) User-visible and user-invisible registers
B) Control and user-invisible registers
C) Control and Status registers
D) User-visible and Control/Status registers

Answer: D

13) When an external device becomes ready to be serviced by the processor the device sends a(n) _____ signal to the processor.

A) access B) halt C) handler D) interrupt

Answer: D

14) One mechanism Intel uses to make its caches more effective is _____ , in which the hardware examines memory access patterns and attempts to fill the caches speculatively with data that is likely to be requested soon.

A) mapping
B) handling
C) interconnecting
D) prefetching

Answer: D

15) A _____ organization has a number of potential advantages over a uniprocessor organization including performance, availability, incremental growth, and scaling.

A) temporal locality B) symmetric multiprocessor
C) direct memory access D) processor status word

Answer: B

**SHORT ANSWER QUESTIONS:**

1) The invention of the _____ was the hardware revolution that brought about desktop and handheld computing.

Answer: microprocessor

2) To satisfy the requirements of handheld devices, the classic microprocessor is giving way to the _____ , where not just the CPUs and caches are on the same chip, but also many of the other components of the system, such as DSPs, GPUs, I/O devices and main memory.

Answer: System on a Chip (SoC)

3) The processing required for a single instruction is called a(n) _____ cycle.

Answer: instruction

4) The fetched instruction is loaded into the _____ .

Answer: Instruction Register (IR)

5) When an external device is ready to accept more data from the processor, the I/O module for that external device sends an _____ signal to the processor.

Answer: interrupt request

6) The _____ is a device for staging the movement of data between main memory and processor registers to improve performance and is not usually visible to the programmer or processor.

Answer: cache

7) External, nonvolatile memory is also referred to as _____ or auxiliary memory.

Answer: secondary memory

8) When a new block of data is read into the cache the _____ determines which cache location the block will occupy.

Answer: mapping function

9) In a _____ multiprocessor all processors can perform the same functions so the failure of a single processor does not halt the machine.

Answer: symmetric

10) A _____ computer combines two or more processors on a single piece of silicon.

Answer: multicore

11) A Control/Status register that contains the address of the next instruction to be fetched is called the _____.

Answer: Program Counter (PC)

12) Each location in Main Memory contains a _____ value that can be interpreted as either an instruction or data.

Answer: binary number

13) A special type of address register required by a system that implements user visible stack addressing is called a _____ .

Answer: stack pointer

14) Registers that are used by system programs to minimize main memory references by optimizing register use are called _____ .

Answer: user-visible registers

15) The concept of multiple programs taking turns in execution is known as _____.

Answer: multiprogramming