Exam

Name_____

TRUE/FALSE. Write 'T' if the statement is true and 'F' if the statement is false.

1) A LOW input to an inverter produces a HIGH output. 1) _____
Answer: True False

2) The OR gate performs a function similar to series-connected switches. 2) _____
Answer: True False

3) The output of an AND gate is HIGH only when all inputs are HIGH. 3) _____
Answer: True False

4) The output of an AND gate is LOW only when all inputs are LOW. 4) _____
Answer: True False

5) When the inputs to a 3-input AND gate are 001, the output is HIGH. 5) _____
Answer: True False

6) When the inputs to a 3-input OR gate are 001, the output is HIGH. 6) _____
Answer: True False

7) The output of an OR gate is HIGH when at least one input is HIGH. 7) _____
Answer: True False

8) The output of an OR gate is LOW when at least one input is LOW. 8) _____
Answer: True False

9) The output of a NAND gate is HIGH only when one or more inputs are HIGH. 9) _____
Answer: True False

10) The output of a NAND gate is LOW only when all inputs are HIGH. 10) _____
Answer: True False

11) The output of a NOR gate is LOW only when all inputs are HIGH. 11) _____
Answer: True False

12) The output of a NOR gate is HIGH only when all inputs are HIGH. 12) _____
Answer: True False

13) When the inputs to a 3-input NAND gate are 001, the output is HIGH. 13) _____
Answer: True False

14) When the inputs to a 3-input NOR gate are 001, the output is LOW. 14) _____
Answer: True False

15) The output of a 2-input Exclusive-OR gate is HIGH when the inputs are equal, or identical. 15) _____

Answer: True False

16) The output of a 2-input Exclusive-NOR gate is HIGH when the inputs are equal, or identical. 16) _____

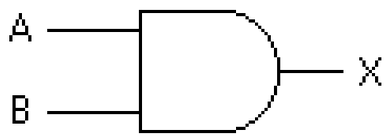
Answer: True False

17) A circle, or "bubble," on a distinctive-shape logic symbol indicates a logic inversion. 17) _____

Answer: True False

MULTIPLE CHOICE. Choose the one alternative that best completes the statement or answers the question.

18) The symbol below represents a(n) _____. 18) _____



A) NAND gate B) AND gate
C) OR gate D) none of the above

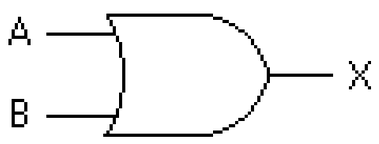
Answer: B

19) The symbol below represents a(n) _____. 19) _____

A) NAND gate B) AND gate
C) OR gate D) none of the above

Answer: B

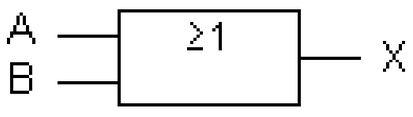
20) The symbol below represents a(n) _____. 20) _____



A) AND gate B) Inverter
C) OR gate D) none of the above

Answer: C

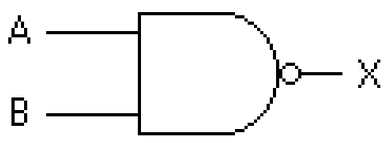
21) The symbol below represents a(n) _____. 21) _____



A) Inverter B) OR gate
C) AND gate D) none of the above

Answer: B

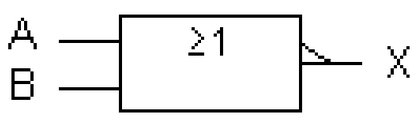
22) The symbol below represents a(n) _____. 22) _____



A) OR gate B) Inverter C) AND gate D) NAND gate

Answer: D

23) The symbol below represents a(n) _____. 23) _____



A) Exclusive-NOR gate B) inverter
C) NOR gate D) NAND gate

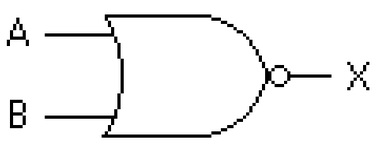
Answer: C

24) The symbol below represents a(n) _____. 24) _____

A) NOR gate B) NAND gate
C) inverter D) Exclusive-NOR gate

Answer: B

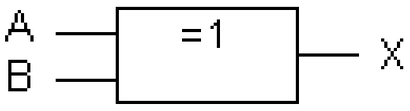
25) The symbol below represents a(n) _____. 25) _____



A) AND gate B) NAND gate C) NOR gate D) OR gate

Answer: C

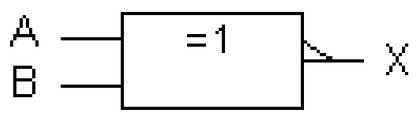
26) The symbol below represents a(n) _____. 26) _____



A) OR gate B) Exclusive-OR gate
C) NAND gate D) AND gate

Answer: B

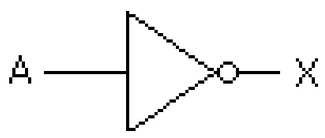
27) The symbol below represents a(n) _____. 27) _____



A) Exclusive-NOR gate B) Exclusive-OR gate
C) NAND gate D) NOR gate

Answer: A

28) The symbol below represents a(n) _____. 28) _____



A) Inverter B) OR gate C) AND gate D) NAND gate

Answer: A

29) The truth table below describes a(n) _____. 29) _____

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

A) AND gate B) OR gate C) NOR gate D) NAND gate

Answer: A

30) The truth table below describes a(n) _____. 30) _____

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

A) AND gate B) OR gate C) NOR gate D) NAND gate

Answer: B

31) The truth table below describes a(n) _____. 31) _____

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

A) AND gate B) OR gate C) NOR gate D) NAND gate

Answer: D

32) The truth table below describes a(n) _____. 32) _____

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

A) AND gate B) OR gate C) NOR gate D) NAND gate

Answer: C

33) Which of the truth tables below describes the Exclusive-NOR gate? 33) _____

A	B	X
0	0	1
0	1	0
1	0	0
1	1	1

(A)

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

(B)

A	B	X
0	0	0
0	1	1
1	0	1
1	1	0

(C)

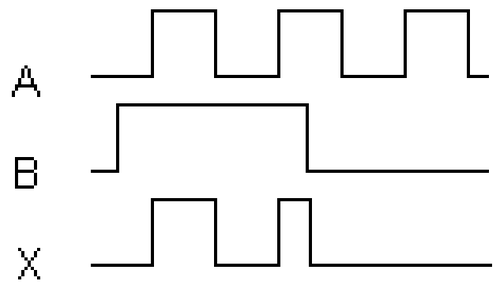
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

(D)

A) (A) B) (B) C) (C) D) (D)

Answer: A

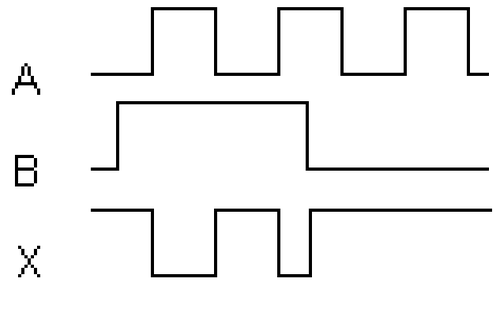
34) The timing diagram below is correct for a 2-input _____ gate. 34) _____



A) AND B) OR C) NAND D) Exclusive-OR

Answer: A

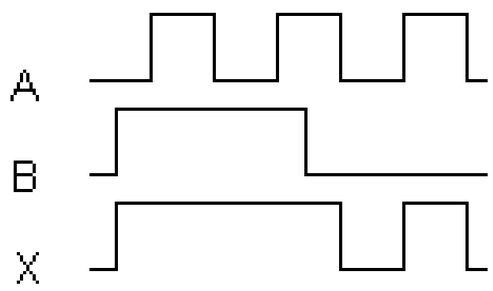
35) The timing diagram below is correct for a 2-input _____ gate. 35) _____



A) AND B) OR C) NAND D) Exclusive-OR

Answer: C

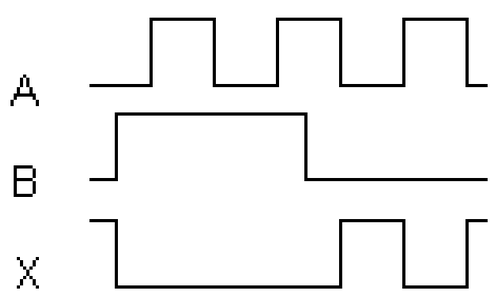
36) The timing diagram below is correct for a 2-input _____ gate. 36) _____



A) AND B) OR C) NAND D) Exclusive-OR

Answer: B

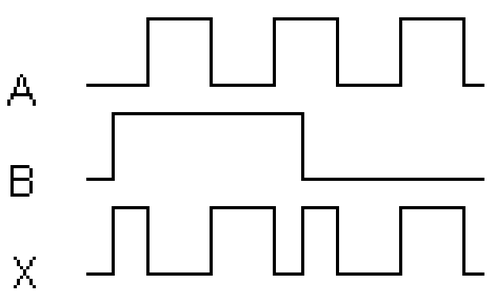
37) The timing diagram below is correct for a 2-input _____ gate. 37) _____



A) AND B) OR C) Exclusive-NOR D) NOR

Answer: D

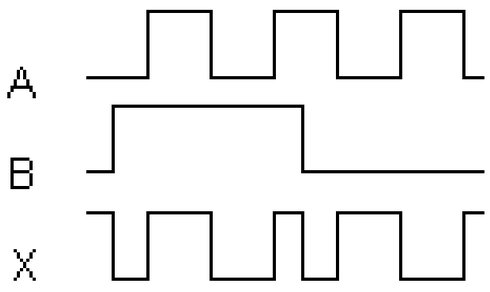
38) The timing diagram below is correct for a 2-input _____ gate. 38) _____



A) NAND B) Exclusive-NOR C) AND D) Exclusive-OR

Answer: D

39) The timing diagram below is correct for a 2-input _____ gate. 39) _____



A) Exclusive-OR B) NAND C) AND D) Exclusive-NOR

Answer: D

40) IC's with a _____ prefix have a broad operating temperature range and are generally used by the military. 40) _____

A) 74 B) TTL C) 2N D) 54

Answer: D

41) The _____ series of IC's are pin, function and voltage-level compatible with the 74 series IC's. 41) _____

A) ALS B) 2N C) HCT D) CMOS

Answer: C

42) A logic gate draws 10mA when its output is HIGH and 20mA when its output is LOW. When operating from a 12V supply with a 10% duty cycle the average power dissipation will be _____. 42) _____

A) 228mW B) 360mW C) 324mW D) 180mW

Answer: A

43) The fanout for standard bipolar logic devices is _____. 43) _____

A) 5 B) 10 C) 2 D) 1

Answer: B

44) The term "hex inverter" refers to _____. 44)

A) six inverters in a single package B) an inverter which has six inputs

C) an inverter that has a history of failure D) a six-input symbolic logic device

Answer: A

45) Which type of gate can be used to add two bits? 45) _____

A) XNAND B) NOR C) NAND D) XOR

Answer: D

46) An AND gate is checked for operation and the following readings are taken on the gate: input A = 0.2 V, input B = 4.5 V, input C = 0.4 V, output = 4.9 V. What might be wrong with the gate? 46) _____

A) Input C is too high. B) The output is stuck high; the chip is bad.

C) The output is too low: it should be 5 V. D) Nothing is wrong with the gate.

Answer: B

47) When an open occurs on the input to a bipolar logic device, the output will _____. 47) _____

A) go LOW, because there is no current in an open circuit

B) go HIGH, since full voltage appears across an open

C) react to the open input as if it were a HIGH input

D) still be good, if only the good inputs are used

Answer: C

48) When an open occurs on the input of a CMOS gate, the output will _____. 48) _____

A) go LOW, because there is no current in an open circuit

B) go HIGH, since full voltage appears across an open

C) be treated as if the open input were a HIGH

D) be unpredictable; it may go HIGH or LOW

Answer: D

49) What technology allows a GAL to be reprogrammed again and again? 49) _____

A) TTL B) CMOS C) E^2CMOS D) NMOS

Answer: C

50) What programmable arrays are in PLD's? 50) _____
A) OR arrays and AND arrays B) OR arrays only
C) AND arrays only D) NOR arrays
Answer: A

51) Which of the following is not a type of SPLD? 51) _____
A) GAL B) RAM C) PLA D) PROM
Answer: B

52) The difference between a PLA and a PAL is _____. 52) _____
A) the PAL has more possible product terms than the PLA
B) the PLA has a programmable OR plane and a programmable AND plane while the PAL only has a programmable AND plane
C) the PAL has a programmable OR plane and a programmable AND plane while the PLA only has a programmable AND plane
D) PALs and PLAs are the same thing.
Answer: B

53) HDL stands for _____. 53) _____
A) hardwire descriptive logic B) hardware description language
C) hardwired digital logic D) none of the above
Answer: B

54) HDLs differ from _____ in that they include ways of describing propagation times and other logic characteristics. 54) _____
A) software programming languages B) software digital logic
C) software description languages D) none of the above
Answer: C

55) The _____ in a VHDL program defines the logic element and its inputs/outputs or ports. 55) _____
A) source B) hardware C) entity D) architecture
Answer: C

56) The _____ in a VHDL program describes its logic operation. 56) _____
A) source B) architecture C) entity D) hardware
Answer: B

57) A _____ IC comes with logic functions that are not programmed in and cannot be altered. 57) _____
A) VHDL B) HDL C) fixed-function D) microcontroller
Answer: C